R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102 as being anticipated by Batchelor, U.S. Patent Publication No. 2004/0025129A1 is respectfully traversed and should be withdrawn.

Batchelor concerns a system and methods for pre-artwork signal-timing verification of an integrated circuit design (Title).

In contrast, claim 1 provides a step for (A) identifying a plurality of clock signals by analyzing a circuit design. Despite the assertion in the Office Action, FIGS. 4 and 6 and the text in paragraph 0061 of Batchelor appear to be silent regarding clock signals. Assuming, *arguendo*, that the clock buffers mentioned in Batchelor suggest clock signals (for which Applicants' representative does not necessarily agree), Batchelor still remains silent that the suggested clock signals are identified by analyzing a circuit design as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests a step for identifying a plurality of clock signals **by analyzing a circuit design** or (ii) withdraw the rejection.

Claim 1 further provides a step for (B) determining a plurality of relationships among the clock signals. Despite the assertion in the Office Action, FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor appear to be silent regarding a step for determining a plurality of relationships among clock signals as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests a step for determining **a plurality of relationships among a plurality of clock signals** or (ii) withdraw the rejection.

Claim 1 further provides a step for (C) generating a plurality of timing constraints for the circuit design in response to the clock signals and the relationships among the clock signals. Despite the assertion in the Office Action, FIG. 6 and the text in paragraphs 0059 and 0063 of Batchelor appear to be silent regarding a step for generating a plurality of timing constraints for a circuit design in response to a plurality of clock signals and a plurality of relationships among the clock signals as presently claimed. Therefore, *prima facie* anticipation has not been established. Claim 20 provides language similar to claim 1. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests a step for generating a plurality of timing constraints for a circuit design **in response to** a plurality of clock signals

and a plurality of relationships among the clock signals or (ii) withdraw the rejection to claims 1 and 20.

Claim 14 provides a step for (A) identifying a plurality of clock signals by analyzing a circuit design. Despite the assertion in the Office Action, FIGS. 4 and 6 and the text in paragraph 0061 of Batchelor appear to be silent regarding clock signals. Assuming, *arguendo*, that the clock buffers mentioned in Batchelor suggest clock signals (for which Applicants' representative does not necessarily agree), Batchelor still remains silent that the suggested clock signals are identified by analyzing a circuit design as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests a step for identifying a plurality of clock signals **by analyzing** a circuit design or (ii) withdraw the rejection.

Claim 14 further provides a step for (B) querying a user for a plurality of parameters for the clock signals. In contrast, the Office Action fails to provide any evidence or arguments against the claimed step. In particular, the arguments against claim 14 only cite the language of claim 1, which is different than the language of claim 14. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) provide a new non-final Office Action with evidence and arguments how Batchelor allegedly anticipates the claimed step or (ii) withdraw the rejection.

Claim 14 further provides a step for (C) generating a plurality of timing constraints in response to a plurality of clock signals and a plurality of parameters. In contrast, the Office Action fails to provide any evidence or arguments against the claimed step. In particular, the arguments against claim 14 only cite the language of claim 1, which is different than the language of claim 14. Therefore, *prima facie* anticipation has not been established. Claim 21 provides language similar to claim 14. As such, the Examiner is respectfully requested to either (i) provide a new non-final Office Action with evidence and arguments how Batchelor allegedly anticipates the claimed step or (ii) withdraw the rejection to claims 14 and 21.

Claim 2 provides that the plurality of clock signals comprise a test clock signal. Despite the assertion in the Office Action, FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor appear to be silent regarding a test clock signal as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests a test clock signal or (ii) withdraw the rejection.

Claim 3 provides a step of eliminating a respective timing constraint of a plurality of timing constraints for each signal connected to an internal pin for a circuit design that defines a non-clock signal. Despite the assertion in the Office Action, FIG. 6 and the text in paragraphs 0060 and 0061 of

Batchelor appear to be silent regarding a step for eliminating from a plurality of timing constraints as presently claimed. Therefore, *prima facie* anticipation has not been established. Claim 4 provides language similar to claim 3. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests a step for eliminating from a plurality of timing constraints or (ii) withdraw the rejections of claims 3 and 4.

Claim 6 provides that at least one of a plurality of parameters relates to a test clock signal. Despite the assertion in the Office Action, the text in paragraphs 0016 and 0064 of Batchelor appear to be silent regarding a test clock signal as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests a test clock signal or (ii) withdraw the rejection.

Claim 7 provides a step for eliminating a respective timing constraint of a plurality of timing constraints for each signal of a circuit design that defines a static signal. In contrast, the Office Action provides no evidence or arguments that Batchelor anticipates the claimed step. In particular, the cites to "fig 1-5 col 2 lines 23-61 and col 3 lines 16 to col 4 lines 64" is a residue from the previous Office Action citing figures and text of Ginetti et al. '658. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully

requested to either (i) provide a new non-final Office Action with evidence and agreements how Batchelor allegedly anticipates the claimed step or (ii) withdraw the rejection.

Claim 8 provides that the step (B) for determining a plurality of relationships among a plurality of clock signals comprises a sub-step of generating an asynchronous relationship of the relationships between at least two of the clock signals operating asynchronously to each other. Despite the assertion in the Office Action, the FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor appear to be silent regarding at least two clock signals operating asynchronously to each other as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests at least two clock signals operating asynchronously to each other or (ii) withdraw the rejection.

Claim 9 provides that the step (B) further comprises a sub-step of generating a fastest clock relationship of the relationships between at least two of the clock signals operating at different speeds between two clock boundaries of the circuit design. Despite the assertion in the Office Action, the FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor appear to be silent regarding at least two clock signals operating at different speeds between two clock boundaries as presently claimed. Therefore, *prima facie* anticipation has not been established. As

such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests at least two clock signals operating at different speeds between two clock boundaries or (ii) withdraw the rejection.

Claim 10 provides that the step (B) further comprises a sub-step of generating a multiplexed clock relationship of the relationships between at least two of the clock signals routable through a multiplexer in the circuit design. Despite the assertion in the Office Action, the FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor appear to be silent regarding at least two of the clock signals routable through a multiplexer as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests (a) a multiplexer and (b) two clock signals routed through the multiplexer or (ii) withdraw the rejection.

Claim 11 provides that the step (B) further comprises a sub-step of generating a derivative clock relationship of the relationships between a first of the clock signals that is derived from a second of the clock signals. Despite the assertion in the Office Action, the FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor appear to be silent regarding a first clock signal derived from a second clock signal as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly

and concisely identify where Batchelor allegedly discloses or suggests a first clock signal derived from a second clock signal or (ii) withdraw the rejection.

Claim 12 provides that the step (B) further comprises a sub-step of generating a shared structure relationship of the relationships between a test clock signal of the clock signals and a normal clock signal of the clock signals, each driving a particular structure of the circuit design in different modes for the circuit design. Despite the assertion in the Office Action, the FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor appear to be silent regarding (a) a shared structure relationship, (b) a test clock signal, (c) a particular structure of a circuit design and (d) different modes as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests (a) a shared structure relationship, (b) a test clock signal, (c) a particular structure of a circuit design and (d) different modes or (ii) withdraw the rejection.

Claim 13 provides a step for writing a plurality of timing constraints among a plurality of files. Despite the assertion in the Office Action, the text in paragraphs 0016 and 0064 of Batchelor appear to be silent regarding writing timing constraints among a plurality of files as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly

and concisely identify where Batchelor allegedly discloses or suggests (a) a plurality of files and (b) a step for writing timing constraints among the files or (ii) withdraw the rejection.

Claim 16 provides a step for querying a user for a frequency parameter for each of the clock signals. Despite the assertion in the Office Action, the text in paragraphs 0016 and 0064 of Batchelor appear to be silent regarding querying a user for parameters as presently claimed. Therefore, *prima facie* anticipation has not been established. Claim 17 provides language similar to claim 16. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly discloses or suggests a step for querying a user or (ii) withdraw the rejections for claims 16 and 17.

COMPLETENESS OF THE OFFICE ACTION

Aside from a notice of allowance, Applicants' representative respectfully requests that any further action on the merits be presented as a non-final action. The Examiner is respectfully requested to refrain from omnibus rejections that simply list all of the claimed elements and then assert that the claimed elements are disclosed somewhere among one or two figures and six paragraphs of text (see MPEP 707.07(d)). Furthermore, 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to

such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

No evidence or arguments were presented directed to claim 14 steps (B) and (C) or claim 7. Therefore, the current Office Action is incomplete.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829

Dated: January 17, 2005

c/o Tim Croll
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

Docket No.: 03-0228 / 1496.00302